Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listings of Claims:

1. (original) A memory card conforming to a first operation standard and a second operation standard, comprising:

a non-volatile semiconductor memory having plural semiconductor memory cells, capable of storing given information, and

a controller that executes operation instructions to the non-volatile semiconductor memory on the basis of commands issued from the outside, wherein:

the controller controls a first data output timing that satisfies the first operation standard and the second operation standard, in a first operation mode, and controls a second data output timing that satisfies the first operation standard, in a second operation mode.

2. (original) The memory card according to Claim 1, wherein:

the controller includes a data timing switching unit that outputs data at a fall edge of a clock signal in the first data output timing, and outputs data at a rise edge of a clock signal in the second data output timing.

3. (original) The memory card according to Claim 2, wherein the data timing switching unit includes:

a timing register to which one of the first data output timing and the second data output timing is set,

a first latch that latches an output data enable signal on the basis of an inverted signal of the clock signal,

a second latch that latches the data on the basis of the inverted signal of the clock signal,

a first selector that inputs the output data enable signal and a first latch signal outputted from the first latch, and selects and outputs one of the output data enable signal and the first latch signal on the basis of a value set to the timing register, and

a second selector that inputs the data and a second latch signal outputted from the second latch, and selects and outputs one of the data and the second latch signal on the basis of a value set to the timing register, and

the data timing switching unit outputs:

the output data enable signal and the data to an output buffer from the first selector and the second selector, respectively, when the first data output timing is set to the timing register, and

the first latch signal and the second latch signal to the output buffer from the first selector and the second selector, respectively, when the second data output timing is set to the timing register, wherein:

the output buffer outputs the data on the basis of the output data enable signal to thereby output the data at the fall edge of the clock signal, outputs the second latch

signal by the first latch signal to thereby output the data at the rise edge of the clock signal, and thereby switches an output timing.

4. (original) The memory card according to Claim 1, wherein:

the controller includes a timing delay switching unit that outputs data at a first delay time at the first data output timing, and outputs the data at a second delay time being shorter than the first delay time at the second data output timing.

5. (original) The memory card according to Claim 4, wherein the timing delay switching unit includes:

a timing register to which one of the first data output timing and the second data output timing is set,

a first delay circuit that delays an output data enable signal by the first delay time,

a second delay circuit that delays the data by the first delay time,

a third delay circuit that delays the output data enable signal by the second delay time,

a fourth delay circuit that delays the data by the second delay time,

a third selector that inputs output data enable signals outputted from the first and second delay circuits, and selects and outputs one of the two output data enable signals on the basis of a value set to the timing register, and

a fourth selector that inputs the data pieces outputted from the first and second delay circuits, and selects and outputs one of the data pieces on the basis of a value set to the timing register, and

the timing delay switching unit outputs:

the output data enable signals and the data delayed by the first and second delay circuits to an output buffer from the third selector and the fourth selector, respectively, when the first data output timing is set to the timing register, and

the output data enable signals and the data delayed by the third and fourth delay circuits to the output buffer from the third selector and the fourth selector, respectively, when the second data output timing is set to the timing register, wherein:

the output buffer outputs the data on the basis of the output data enable signal, and thereby switches the output timing.

6. (original) The memory card according to Claim 1, wherein:

the controller includes a data output time switching unit that switches a rise time/fall time of the data in the first data output timing, so that the rise time/fall time of the data becomes shorter to the first data output timing.

7. (original) The memory card according to Claim 6, wherein the data output time switching unit includes:

a timing register to which one of the first data output timing and the second data output timing is set,

an output buffer that outputs data on the basis of an output data enable signal, when one of the first data output timing and the second data output timing is set to the timing register,

an auxiliary output buffer that outputs data on the basis of the output data enable signal at the second data output timing, and

an auxiliary output buffer enable unit that outputs the output data enable signal to the auxiliary output buffer, when the second data output timing is set to the timing register.

8. (original) The memory card according to Claim 6, wherein the data output time switching unit includes:

a timing register to which one of the first data output timing and the second data output timing is set,

an output buffer that outputs data on the basis of an output data enable signal, when one of the first data output timing and the second data output timing is set to the timing register,

plural auxiliary output buffers that output data on the basis of the output data enable signal at the second data output timing, and

an auxiliary output buffer enable unit that outputs the output data enable signal to an arbitrary auxiliary output buffer of the plural auxiliary output buffers in correspondence with a power consumption parameter set to a

power consumption parameter register, when the second data output timing is set to the timing register.

9. (currently amended) The memory card according to ~~any one of~~ Claim 1 ~~through Claim 8~~, wherein the controller includes:

the power consumption parameter register to which are set power consumption parameters that specify power consumptions,

a clock generator that generates a clock signal of an arbitrary frequency,

plural frequency dividers that output to divide the frequency of the clock signal generated by the clock generator into different frequencies, and

a system clock selector that selects any one clock signal among the clock signal and plural clock signals outputted from the plural frequency dividers on the basis of the parameter value set to the power consumption parameter register, and supplies the one selected as a system clock, wherein:

the system clock selector selects the system clock of a higher frequency, as the power consumption parameter becomes a value lager than a default value corresponding to the minimum power consumption.

10. (currently amended) The memory card according to ~~any one of~~ Claim 1 ~~through Claim 9~~, wherein, when plural non-volatile semiconductor memories are provided, the controller controls the plural non-volatile semiconductor memories arbitrarily in parallel operation in

correspondence with the parameter value set to the power consumption parameter register.

Claims 11-14 (cancelled).